IV. Claims

Claims 1-23 are currently pending. Claims 1-4, 6, 9, 10-11, 13-14, 16 and 17-21 are amended as set for the below. Claims 5 and 15 have been canceled. New Claims 24-29 have been added. This listing replaces all prior listings and versions of the claims.

1. (currently amended) A digital phase lock loop circuit for recovering a sampling clock comprising:

an error generation circuit for generating at least three error signals from a sampled signal; and,

a phase error adjustment circuit for generating at least first and second ~~one~~ phase error adjustment signals from the at least three error signals for adjusting for at least an amount and direction of occurring phase drift, respectively, of a recovered sampling clock.

2. (currently amended) The digital phase lock loop circuit of claim 1, wherein the at least three error signals comprise:

at least one first error signal, said first error signal corresponding to an error between a first sampled value from said sampled signal and a first ideal value for said sampled signal;

at least one second error signal, said second error signal corresponding to an error between a second sampled value from said sampled signal, slightly ahead of the first sampled value in time, and the first ideal value; and,

at least one third error signal, said third error signal corresponding to an error between a third sampled value from said sampled signal, slightly behind the first sampled

value in time, and the first ideal value.

3. (currently amended) The digital phase lock loop circuit of claim 1, wherein the at least three error signals comprise:

at least one first error signal, said first error signal corresponding to an error between a first sampled value from said sampled signal and a first ideal value for said sampled waveform;

at least one second error signal, said second error signal corresponding to an error between a first interpolated sample value for said sampled signal, slightly ahead of the first sampled value in time, and the first ideal value; and,

at least one third error signal, said third error signal corresponding to an error between a second interpolated sample value for said sampled signal, slightly behind the first sampled value in time, and the first ideal value.

4. (currently amended) The digital phase lock loop circuit of claim 1, wherein the at least three error signals comprise:

at least one first error signal, said first error signal corresponding to an error between a first sampled value from said sampled signal and a first ideal value for said sampled signal;

at least one second error signal, said second error signal corresponding to an error between the first sampled value and a second ideal value for said sampled signal which is slightly ahead of the first ideal value in time; and,

at least one third error signal, said third error signal corresponding to an error between the first sampled value and a third ideal value for said sampled signal which is

slightly behind the first ideal value in time.

5. (canceled)

6. (currently amended) The digital phase lock loop circuit of claim 4, wherein the at least one first error signal is produced by taking the difference between a first digital output signal corresponding to said sampled signal and a second digital output signal corresponding to said first ideal value.

7. (original) The digital phase lock loop circuit of claim 6, wherein the at least one second error signal is produced by taking the difference between the first digital output signal and a phase shifted version of the second digital output signal, said phase shift being in a positive direction.

8. (original) The digital phase lock loop circuit of claim 6, wherein the at least one second error signal is produced by taking the difference between the first digital output signal and a phase shifted version of the second digital output signal, said phase shift being in a negative direction.

9. (currently amended) The digital phase lock loop circuit of claim 1, wherein the at least first and second ~~one~~ phase error adjustment signals further comprises ~~at least three signals including:~~

~~at least one drift direction signal~~

at least one drift duration signal~~; and~~

~~at least one drift amount signal~~.

10. (currently amended) A read channel device comprising:

an error generation circuit for generating at least three error signals from a sampled signal; and,

a phase error adjustment circuit for generating at least first and second ~~one~~ phase error adjustment signals from the at least three error signals for adjusting for at least an amount and direction of occurring phase drift, respectively, of a recovered sampling clock.

11. (currently amended) A data storage system comprising:

a data storage assembly;

a read channel device operable to read information stored on the data storage assembly, said read channel device comprising an error generation circuit for generating at least three error signals from a sampled signal; and, a phase error adjustment circuit for generating at least first and second ~~one~~ phase error adjustment signals from the at least three error signals indicative of at least an amount and direction of occurring phase drift, respectively, of a recovered sampling clock.

12. (original) The data storage system of claim 11, wherein said data storage assembly comprises a hard disk drive.

13. (currently amended) A method for determining and correcting a phase error in a recovered sampling clock, comprising the steps of:

generating at least three error signals from a sampled signal; and,

generating at least first and second ~~one~~ phase error adjustment signals from the at least three error signals for adjusting for at least an amount and direction of occurring phase drift, respectively, of said recovered sampling clock.

14. (currently amended) The method of claim 13, wherein the step of generating at least three error signals comprises:

generating at least one first error signal, said first error signal corresponding to an error between a first sampled value from said sampled signal and a first ideal value for the sampled signal;

generating at least one second error signal, said second error signal corresponding to an error between the first sampled value and a second ideal value for the sampled signal which is slightly ahead of the first ideal value in time; and,

generating at least one third error signal, said third error signal corresponding to an error between the first sampled value and a third ideal value for the sampled signal which is slightly behind the first ideal value in time.

15. (canceled)

16. (currently amended) The method of claim 14 ~~15~~, wherein the step of generating the at least first and second ~~one~~ phase error adjustment signals comprises the further steps of:

generating at least one drift duration signal~~; and,~~

~~generating at least one drift amount signal~~.

17. (currently amended) The method of claim 14 ~~13~~, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the sum of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the sum of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the sum of a plurality of the at least one third error signals.

18. (currently amended) The method of claim 14 ~~13~~, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the root mean square of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the root mean square of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the root mean square of a plurality of the at least one third error signals.

19. (currently amended) The method of claim 14 ~~13~~, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the sum of the squares of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the sum of the squares of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the sum of the squares of a plurality of the at least one third error signals.

20. (currently amended) The method of claim 14 ~~13~~, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the mean sum of the squares of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the mean sum of the squares of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the mean sum of the squares of a plurality of the at least one third error signals.

21. (currently amended) The method of claim 14 ~~13~~, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the absolute sum of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the absolute sum of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the absolute sum of a plurality of the at least one third error signals.

22. (original) The method of claim 17, comprising the further step of:

determining if the at least one third summation error signal is less than both the at least one first summation error signal and the at least one second summation error signal;

and,

generating a phase error adjustment signal which is positive, if the at least one third summation error signal is less than both the at least one first summation error signal and the at least one second summation error signal.

23. (original) The method of claim 17, comprising the further step of:

determining if the at least one second summation error signal is less than both the at least one first summation error signal and the at least one third summation error signal; and,

generating a phase error adjustment signal which is negative, if the at least one second summation error signal is less than both the at least one first summation error signal and the at least one third summation error signal.

24. (new) The digital phase lock loop of claim 1, further comprising an oscillator for generating said sampling clock, said oscillator responsive to a control signal for countering said occurring drift responsive to said at least one phase error adjustment signal.

25. (new) A digital phase lock loop circuit for recovering a sampling clock, comprising:

an error generation circuit for generating at least three error signals from a sampled signal sampled with said sampling clock, said at least three error signals comprising:

at least one first error signal, said first error signal corresponding to an error between a first sampled value from said sampled signal and a first ideal value for said sampled signal;

at least one second error signal, said second error signal corresponding to an error between a second sampled value from said sampled signal, slightly ahead of the first sampled

value in time, and the first ideal value; and

at least one third error signal, said third error signal corresponding to an error between a third sampled value from said sampled signal, slightly behind the first sampled value in time, and the first ideal value; and

a phase error adjustment circuit for generating at least one phase error adjustment signal from the at least three error signals.

26. (new) A digital phase lock loop circuit for recovering a sampling clock, comprising:

an error generation circuit for generating at least three error signals from a sampled signal sampled with said sampling clock, said at least three error signals comprising:

at least one first error signal, said first error signal corresponding to an error between a first sampled value from said sampled signal and a first ideal value for said sampled waveform;

at least one second error signal, said second error signal corresponding to an error between a first interpolated sample value for said sampled signal, slightly ahead of the first sampled value in time, and the first ideal value; and,

at least one third error signal, said third error signal corresponding to an error between a second interpolated sample value for said sampled signal, slightly behind the first sampled value in time, and the first ideal value; and

a phase error adjustment circuit for generating at least one phase error adjustment signal from the at least three error signals.

27. (new) A digital phase lock loop circuit for recovering a sampling clock, comprising:

an error generation circuit for generating at least three error signals from a sampled signal

sampled with said sampling clock, said at least three error signals comprising:

at least one first error signal, said first error signal corresponding to an error between a first sampled value from said sampled signal and a first ideal value for said sampled signal;

at least one second error signal, said second error signal corresponding to an error between the first sampled value and a second ideal value for said sampled signal which is slightly ahead of the first ideal value in time; and,

at least one third error signal, said third error signal corresponding to an error between the first sampled value and a third ideal value for said sampled signal which is slightly behind the first ideal value in time; and

a phase error adjustment circuit for generating at least one phase error adjustment signal from the at least three error signals.

28. (new) The digital phase lock loop of claim 1, wherein the second phase error adjustment signal indicates a direction opposite said direction of said occurring phase drift.

29. (new) The method of claim 13, wherein the second phase error adjustment signal indicates a direction opposite said direction of said occurring phase drift.